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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,205	01/26/2004	Nobuaki Hashimoto	118212	6430

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EXAMINER	
PAREKH, NITIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/763,205	HASHIMOTO, NOBUAKI
	Examiner	Art Unit
	Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3 and 9, 10 and 12-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakamura et al. (US Pat. 6784557).

Regarding claims 1, 10, 12 and 14, Nakamura et al. teach a semiconductor device/an electronic device and a method of method of manufacturing such device, comprising:

- a semiconductor substrate/wafer that includes an active element and an integrated circuit/IC chip (11 in Fig. 10C) having an active element in the active element region (see the region under 21 between 12 in Fig. 10C)
- electrodes electrically connected to the integrated circuit, the electrodes including a first electrode and a second electrode (see 12 on left and right sides in Fig. 10C respectively)
- a resin layer (17 in Fig. 10C) that is formed on a surface of the semiconductor substrate where the electrode is also formed, so as to avoid the electrodes

- a wiring layer that extends from the electrode and across a top of the resin layer, and includes a plurality of electrically connecting portions/wiring sections (see 14 connecting respective electrodes in Fig. 10C), the plurality of electrically connecting portions including a first electrically connecting portion electrically connected to the first electrode and a second electrically connecting portion electrically connected to the second electrode, and
- an external terminal (21 in Fig. 10C) that is provided on the electrically connecting portions

(Fig. 9A-10c; Col. 17, line 55- Col. 20, line 15).

Nakamura et al. further teach a conventional electrode/wiring configuration wherein the first and the second electrically connecting portions/wiring sections have different wiring lengths/areas (see 4 having different wiring lengths/areas in Fig. 15A) such that the surface area of the first electrically connecting portion is larger than that of the second electrically connecting portion (Col. 1 and 2).

Regarding claims 2, 3, 9 and 13, Nakamura et al. teach the entire claimed structure as applied to claim 1, wherein Nakamura teach:

- a portion of the second electrically connecting portion being formed on the top surface of the resin layer (see 14 and 17 in Fig. 10C)

- the resin layer (see 17 in Fig. 10C) overlapping the active element region of the semiconductor substrate
- the first electrically connecting portion being formed on the area of the resin layer (see 14 and 17 in Fig. 10C) that overlaps the active element region
- an insulating layer (15 in Fig. 10C) being formed so as to cover the wiring layer while avoiding the external terminal, and
- the IC device comprising a conventional mounting substrate/circuit board (Col. 11, line 67).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4-8 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. (US Pat. 6784557) in view of Shimizu et al. (US Pat. 2001/0000116).

Regarding claims 4-8, Nakamura et al. teach substantially the entire claimed structure as applied to claim 1 including the first electrically connecting portion being formed so

as to further cover a side surface of the resin and extending to the region of the substrate beyond the resin layer (see 14 on the left side in Fig. 10C), but fail to teach the first electrically connecting portion being formed so as to cover nearly the entire top surface of the resin layer.

Shimizu et al. teach a device structure comprising electrode/external terminal connections (see Fig. 1, 7, 16, etc.) having a variety of wiring configurations including the configurations (see Fig. 7 and 16) wherein the first electrically connecting portion/ground wiring section (see ground wiring section 1003 in Fig. 7, also 5003 in Fig. 17) nearly/substantially covers the entire top surface of an underlying insulating/dielectric layer except the for the area occupied by the second electrically connecting portion/wiring section and a portion surrounding the second electrically connecting portion/wiring section (see Fig. 7; sections 0052-0055, 0065 and 0066). Furthermore, such electrically connecting portion/ground wiring section being conventionally formed of different shape/area/size to provide the desired/predetermined electrical performance/characteristics and noise reduction (Col. 5-8).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first electrically connecting portion/ground wiring section being formed so as to cover nearly the entire top surface of the resin layer as taught by Shimizu et al. so that the desired electrical signal requirements/ performance/characteristics and the noise reduction can be achieved in Nakamura et al's device.

Regarding claim 11, Nakamura et al. and Shimizu et al. teach substantially the entire claimed structure as applied to claims 1 and 4 above.

Response to Arguments

5. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Steven Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have

questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

09-13-05

NITIN PAREKH

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800